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5182633, Video sample rate converter, January, 1993, Antonio et al. ... said means for forming the second phase signal includes a second counter which ...
www.freepatentsonline.com/5285263.html - Similar pages - Note this
by T Fujita - 1994 - Cited by 1 - Related articles - All 2 versions

Asynchronous sample rate converter and method - Patent 7262716
The asynchronous sample rate converter of claim 4 wherein the address generation circuitry includes: a second counter clocked by the input sample rate clock ...
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by X Yu - 2007 - Related articles - All 2 versions
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Method and system for sampling rate conversion in digital audio ...
a third variable to store the first counter, a fourth variable to store a second counter to track the samples of the first digital audio signal, and ...
www.patentstorm.us/patents/6509850-claims.html - Similar pages - Note this

Asynchronous sample rate converter and method - US Patent 7262716
An asynchronous sample rate converter interpolates and filters a digital ... a first adder (69) combining the digital output of the second counter (65) with ...
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Inventors Thomas C. Savell, Santa Cruz CA David Rossum, Monterey ...
The apparatus of claim 1 wherein the first counter, second counter or third counter is an ... sample rate of an asynchronous digital sample rate converter. ...
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Inventors Seiichi Mizukoshi, Kanagawa (JP) Tomonori Satoh, Tokyo ...
b. a first counter supplied with said synchronization signal for frame scanning and counting the same;. c. a second counter supplied with said clock signals ...
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A receiver includes a sample rate converter configured to receive an input links includes a first counter that generates a first local network clock, ...
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Multiplex communications inventions April - patents by class relation
Freshpatents.com offers information on a variety of new patent applications, updated each week - check out Multiplex communications inventions April ...
www.freshpatents.com/Multiplex-communications-dt200704ntc370.php - 412k - Cached - Similar pages - Note this

Message routing through data communication networks

Message routing through data communication networks. 4645874. Abstract. A mechanized system distributing the access, test and communication functions to the ...
www.palmerpatent.com/.../4645874_message_routing_through_communication_networks.html - 443k - Cached - Similar pages - Note this

Asynchronous digital sample rate converter - Google Patents Result

US Pat. 5475628 - Analog Devices, Inc.
Asynchronous digital sample rate converter ... and a terminal count output which indicates overflow of the output of the first counter; a second counter ...
www.google.com/patents?id=WjYcAAAAEBAJ

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Asynchronous sample rate tracker - Patent 6324235
The apparatus of claim 1 wherein the first counter, second counter or third A synchronous sample rate converter shares a common time base, or clock, ...
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by TC Savell - 2001 - Cited by 4 - Related articles - All 3 versions

> Asynchronous sample rate estimation using reciprocal frequency ...
> The apparatus of claim 1, further comprising a sample rate converter circuit ... wherein the first counter and the second counter is an overflow buffer. ...
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> Systems and methods for clock mode determination utilizing ...
> 4A, a first counter 401a counts periods of the MCK signal and a second counter 401b counts periods of the FIXCLK signal. The resulting count values ...
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Asynchronous sample rate tracker - Patent Review 6324235
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> Asynchronous sample rate estimation using reciprocal frequency ...
> The apparatus of claim 9, wherein the first counter and the second counter is an overflow buffer. 14. The apparatus of claim 1, wherein the input sample ...
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1. Synchronization of fractional interval counter in non-integer ratio sampl
Ketola, J.; Vankka, J.; Halonen, K.;
Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 Internationa
Volume 2, 25-28 May 2003 Page(s):II-89 - II-92 vol.2
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1. Asynchronous sample rate tracker
Savell, Thomas C. / Rossum, David (Creative Technology, Lt
PATENT AND TRADEMARK OFFICE GRANTED PATENT, Nov 2001
patno:US6324235
...I. Overview of the Sample Rate Converter The present inventi
sample rate converter. An asynchronous sample rate converte
digital...that convert a first digital data stream to another digita
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2. Asynchronous sample rate estimation using reciprocal frequency er
Savell, Thomas C. (Creative Technology Ltd.), *UNITED STATES
OFFICE GRANTED PATENT*, Nov 2004
patno:US6819732
...operating as an asynchronous sample rate converter, or is use
convert a first digital data stream to another digital data strea
asynchronous sample rate converter according to an embodimer
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3. VOICE GATEWAY WITH DOWNSTREAM VOICE SYNCHRONIZATION
RABENKO, Theodore F. / HARTMAN, David / THI, James, C.,
Corporation), *EUROPEAN PATENT*, Sep 2002
patno:EP1238489
...patcit> discloses the use of a sample rate converter (SRC) rec
stream at a first sample rate, outputting the...sample rate. The sa
rate converter is controlled depending on the fill...
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4. Systems and methods for clock mode determination utilizing hyste
Duewer, Bruce Eliot / Melanson, John Laurence (Cirrus Logi
PATENT AND TRADEMARK OFFICE GRANTED PATENT, May 2008
patno:US7379834
...200 including a sample rate converter (SRC) 201; also...fsi,) c
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at...shown in FIG. 4A, a first counter 401a counts periods...MCK s
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6. Systems and methods for clock mode determination utilizing divide
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patno:US7286069
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at...shown in FIG. 4A, a first counter 401a counts periods...MCK s
counter 401b counts periods...
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7. Systems and methods for clock mode determination utilizing a fixe

Duewer, Bruce Eliot / Melanson, John Laurence (Cirrus Logi
PATENT AND TRADEMARK OFFICE GRANTED PATENT, May 2006
patno:US7049988
...200 including a sample rate converter (SRC) 201; also...fsi,) c
stream (INPUT DATA) provided...202 to an output digital data st
at...shown in FIG. 4A, a first counter 401a counts periods...MCK s
counter 401b counts periods...
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8. Systems and methods for clock mode determination utilizing opera measurement
Duewer, Bruce Eliot / Melanson, John Laurence (Cirrus Logi
PATENT AND TRADEMARK OFFICE GRANTED PATENT, Jun 2007
patno:US7236109
...200 including a sample rate converter (SRC) 201; also...fsi,) c
stream (INPUT DATA) provided...202 to an output digital data st
at...shown in FIG. 4A, a first counter 401a counts periods...MCK s
counter 401b counts periods...
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9. Systems and methods for clock mode determination utilizing explic tables
Duewer, Bruce Eliot / Melanson, John Laurence (Cirrus Logi
PATENT AND TRADEMARK OFFICE GRANTED PATENT, Jun 2006
patno:US7057539
...200 including a sample rate converter (SRC) 201; also...fsi,) c
stream (INPUT DATA) provided...202 to an output digital data st
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	Title	Pub. Date	Int. Class	App. Num	Applicant
1.	(WO 2001/043334) VOICE GATEWAY WITH DOWNSTREAM VOICE SYNCHRONIZATION	14.06.2001	E05C 1/00	PCT/US2000/033765	BROADCOM CORPORAT

A network gateway is configured to facilitate on line and off line bi-directional communication between a number of near er telephony devices with far end data termination devices via a hybrid fiber coaxial network and a cable modem termination described network gateway combines a QAM receiver, a transmitter, a DOCSIS MAC, a CPU, a voice and audio processo synchronizer, an Ethernet MAC, and a USB controller to provide high performance and robust operation.

Search Summary

WO/2001/43334: 1 occurrence in 1 record.

Search Time: 0.62 seconds.

VOICE GATEWAY WITH DOWNSTREAM VOICE SYNCHRONIZATION

Publication number: EP1238489

Publication date: 2002-09-11

Inventor: RABENKO THEODORE F (US); HARTMAN DAVID (US); THI JAMES C H (US)

Applicant: BROADCOM CORP (US)

Classification:

- international: *H04B3/23; H04J3/06; H04L12/28; H04L29/06; H04M7/00; H04N7/24; E05C1/00;* H04B3/23; H04J3/06; H04L12/28; H04L29/06; H04M7/00; H04N7/24; E05C1/00; (IPC1-7): H04L7/04; H04J3/06; H04M7/00; H04N7/173

- European: H04L29/06M2S1; H04B3/23; H04B3/23D; H04J3/06B6; H04J3/06C1; H04L12/28B; H04L29/06C2; H04M7/00B2; H04N7/24A

Application number: EP20000984300 20001213

Priority number(s): WO2000US33765 20001213; US19990170592P 19991213; US19990170595P 19991213

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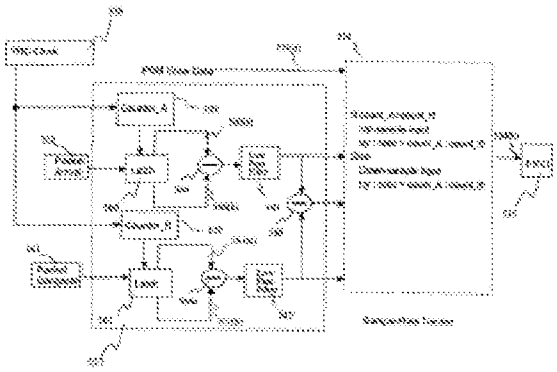
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EP1238489 (A0)

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Abstract of corresponding document: WO0143334

A network gateway is configured to facilitate on line and off line bi-directional communication between a number of near end data and telephony devices with far end data termination devices via a hybrid fiber coaxial network and a cable modem termination system. The described network gateway combines a QAM receiver, a transmitter, a DOCSIS MAC, a CPU, a voice and audio processor, a voice synchronizer, an Ethernet MAC, and a USB controller to provide high performance and robust operation.



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- operating mode
- signal generation
- mode selection
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1. Asynchronous sample rate converter and method
Yu, Xianggang / Sculley, Terry L. / Chang, Jung-Kuei (Texas Incoporated), *UNITED STATES PATENT AND TRADEMARK OFFICE* 2007
patno:US7262716
...described embodiment of the asynchronous sample rate conve invention as shown...1:16 to 16:1. Thus, asynchronous sample ra capability of converting...Greatly simplified, an asynchronous samp considered to include only...
Full text available at patent office. For more in-depth search similar results

2. Asynchronous digital sample rate converter
Adams, Robert W. / Coln, Michael / Kwan, Tom W. (ANALOG INCORPORATED), *EUROPEAN PATENT APPLICATION*, May 1997
patno:EP774835
...particularly, the invention is a sample rate converter capable c sequence...recorders, and similar devices, need a sample rate co audio signals sample...purpose of an asynchronous digital sample decouple the sampling rate...
Full text available at patent office. For more in-depth search similar results

3. Asynchronous sample rate converter and method
Yu, Xianggang / Sculley, Terry L. / Chang, Jung-Kuei (TEXAS INCORPORATED), *UNITED STATES PATENT AND TRADEMARK OF PUBLICATION*, Jun 2004
patno:US20040120361
...described embodiment of the asynchronous sample rate conve invention as shown...1:16 to 16:1. Thus, asynchronous sample ra capability of converting...Greatly simplified, an asynchronous samp considered to include only...
Full text available at patent office. For more in-depth search similar results

4. ASYNCHRONOUS DIGITAL SAMPLE RATE CONVERTER
ADAMS, Robert W. / KWAN, Tom W. / COLN, Michael (Analo *EUROPEAN PATENT*, Jul 1995
patno:EP663118
...particularly, the invention is a sample rate converter capable c sequence...recorders, and similar devices, need a sample rate co audio signals sample...purpose of an asynchronous digital sample decouple the sampling rate...
Full text available at patent office. For more in-depth search similar results

5. Asynchronous digital sample rate converter
Adams, Robert W. / Kwan, Tom W. / Coln, Michael (Analog D *STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Dec
patno:US5475628
...modifications may be made to optimize the sample rate conver applications. The...described above, in order to design a sample ra digital interpolation...For the preferred embodiment a sample rate accuracy was desired...
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6. Asynchronous sample rate tracker
Savell, Thomas C. / Rossum, David (Creative Technology, Lt
PATENT AND TRADEMARK OFFICE GRANTED PATENT, Nov 2001
patno:US6324235
...PREFERRED EMBODIMENT) I. Overview of the Sample Rate Cor
invention provides a...would be provided to an asynchronous samp
asynchronous sample rate converter may be used in a digital au
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7. Sample rate converter for digital video signals having reduced phas
coincidence
Fujita, Tadao (Sony Corporation), *UNITED STATES PATENT ANI*
GRANTED PATENT, Feb 1994
patno:US5285263
A digital video signal processing device is capable of avoid phase d
case of converting the rate of digital video signals. In case of conve
signal to the second digital video signal, the sync ...
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8. Asynchronous sample rate estimation using reciprocal frequency er
Savell, Thomas C. (Creative Technology Ltd.), *UNITED STATES*
OFFICE GRANTED PATENT, Nov 2004
patno:US6819732
...processor operating as an asynchronous sample rate converte
which...electronic devices. An asynchronous sample rate convert
embodiment of the...example, 180° out of phase. In a sample rat
example, if the...
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9. Systems and methods for clock mode determination utilizing hyste
Duewer, Bruce Eliot / Melanson, John Laurence (Cirrus Logi
PATENT AND TRADEMARK OFFICE GRANTED PATENT, May 2008
patno:US7379834
...processing system 200 including a sample rate converter (SRC
describing...embodiment shown in FIG. 4A, a first counter 401a c
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10. Systems and methods for clock mode determination utilizing priorit
Duewer, Bruce Eliot / Melanson, John Laurence / Nanda, Ka
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...processing system 200 including a sample rate converter (SRC
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- frequency ratio
- operating mode
- signal generation
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11. VOICE GATEWAY WITH DOWNSTREAM VOICE SYNCHRONIZATION
RABENKO, Theodore F. / HARTMAN, David / THI, James, C., Corporation), *EUROPEAN PATENT*, Sep 2002
patno:EP1238489
...text> discloses the use of a sample rate converter (SRC) recei stream at a first...stream at a second sample rate. The sampling ra converter is controlled depending on the fill state of the buffer...
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12. Systems and methods for clock mode determination utilizing divide
Duewer, Bruce Eliot / Melanson, John Laurence / Nanda, Ka *UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATE*
patno:US7286069
...processing system 200 including a sample rate converter (SRC describing...embodiment shown in FIG. 4A, a first counter 401a c signal and a second counter 401b counts periods of the FIXCLK...
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13. Systems and methods for clock mode determination utilizing a fixe

Duewer, Bruce Eliot / Melanson, John Laurence (Cirrus Logi *PATENT AND TRADEMARK OFFICE GRANTED PATENT*, May 2006
patno:US7049988
...processing system 200 including a sample rate converter (SRC describing...embodiment shown in FIG. 4A, a first counter 401a c signal and a second counter 401b counts periods of the FIXCLK...
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14. Systems and methods for clock mode determination utilizing opera measurement
Duewer, Bruce Eliot / Melanson, John Laurence (Cirrus Logi *PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Jun 2007
patno:US7236109
...processing system 200 including a sample rate converter (SRC describing...embodiment shown in FIG. 4A, a first counter 401a c signal and a second counter 401b counts periods of the FIXCLK...
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15. Systems and methods for clock mode determination utilizing explic tables
Duewer, Bruce Eliot / Melanson, John Laurence (Cirrus Logi *PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Jun 2006
patno:US7057539
...processing system 200 including a sample rate converter (SRC describing...embodiment shown in FIG. 4A, a first counter 401a c signal and a second counter 401b counts periods of the FIXCLK...
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16. CIRCUITS, SYSTEM, AND METHODS FOR PROCESSING MULTIPLE D
NORTH, Gregory, Allen / GEPHARDT, Douglas / BARNETTE, .

James D. / HABAN, Scott, Thomas / DAVID, Thomas, Sarosh
Christopher (CIRRUS LOGIC, INC.), *PATENT COOPERATION TRI*
1998
patno:WO9835301
An audio information processing subsystem (200) is disclosed whic
processor (100) for simultaneously processing multiple streams of
subsystem (200) also includes a program memory (202) coupled t
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	Title	Pub. Date	Int. Class	App. Num	App
1.	(WO 1998/035301) CIRCUITS, SYSTEM, AND METHODS FOR PROCESSING MULTIPLE DATA STREAMS	13.08.1998	G10H 7/00	PCT/US1998/002319	CIRI INC.

An audio information processing subsystem (200) is disclosed which includes a stream processor (100) for simultaneously multiple streams of audio data. Processing subsystem (200) also includes a program memory (202) coupled to stream pro for storing instructions for controlling processing system (200) and a data memory (203/204) also coupled to stream proce Additionally, a direct memory access circuitry (208) is provided for controlling direct memory accesses to a selected one of memory (202) and data memory (203/204).

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10805591, filed 03/19/2004
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Claims Priority from Provisional Application 60456430, filed 03/21/2003
Claims Priority from Provisional Application 60456429, filed 03/21/2003
Claims Priority from Provisional Application 60456421, filed 03/21/2003

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Application Number Information

Application Number: 10/805591
Assignments

Examiner Number: 80488 / TORRES, JUAN

Filing or 371(c) Date: 03/19/2004 eDan

Group Art Unit: 2611

IFW Madras

Effective Date: 03/19/2004

Class/Subclass: 375/355.000

Application Received: 03/22/2004

Lost Case: NO

Waiting for Response Desc.

Patent Number:

Interference Number:

Amndt.aftr final

Issue Date: 00/00/0000

Unmatched Petition: NO

Date of Abandonment: 00/00/0000

L&R Code: Secrecy Code:1

Attorney Docket Number: D2A1240-1

Third Level Review: NO

Secrecy Order: NO

Status: 80 /RESPONSE AFTER FINAL ACTION FORWARDED TO EXAMINER

Status Date: 08/22/2008

Confirmation Number: 9251

Oral Hearing: NO

Title of Invention: SYSTEMS AND METHODS FOR SAMPLE RATE CONVERSION USING MULTIPLE RATE ESTIMATE COUNTERS

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IDS Flag Clearance for Application 10805591

IDS Information

Content	Mailroom Date	Entry Number	IDS Review	Last Modified	Reviewer
Update					

Inventor Information for 10/805591

Inventor Name	City	State/Country
CHIENG, DANIEL L. W.	AUSTIN	TEXAS
ANDERSEN, JACK B.	AUSTIN	TEXAS
HAND, LARRY E.	MERIDIAN	MISSISSIPPI

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Inventor Name Search Result

Your Search was:

Last Name = CHIENG
First Name = DANIEL

Application#	Patent#	Status	Date Filed	Title	Inventor Name
60755560	Not Issued	159	12/30/2005	Systems amd methods for power supply tracking	CHIENG, DANIEL
60771146	Not Issued	159	02/07/2006	PWM feedback/feed-forward protection	CHIENG, DANIEL
60771147	Not Issued	159	02/07/2006	Full bridge PWM feedback analog input filter component mismatch correction	CHIENG, DANIEL
60771212	Not Issued	159	02/07/2006	Power supply feed forward analog input filter component mismatch correction	CHIENG, DANIEL
60969608	Not Issued	20	09/01/2007	Systems and Methods for HDA Codec with Integrated Class-D PWM Controller to Handle HDA Volume Control	CHIENG, DANIEL L.
60969609	Not Issued	20	09/01/2007	HDA Communication between the Application and the DSP in a HDA Audio Codec for Local Intelligent Processing	CHIENG, DANIEL L.
60969610	Not Issued	20	09/01/2007	DSP Responses to Unsupported Verbs in a HDA Audio Codec to Extend Existing Features or to Implement New Features	CHIENG, DANIEL L.
60969611	Not Issued	20	09/01/2007	Booting over the High Definition Audio Bus	CHIENG, DANIEL L.
60969612	Not Issued	20	09/01/2007	Using DSP to Override Verb Responses to Reconfigure the HDA Audio Codec	CHIENG, DANIEL L.
60969613	Not Issued	20	09/01/2007	Standalone HDA Audio Codec With Integrated Class-D PWM Controller/Amplifier That Has The Ability To Shadow Other HDA Codecs	CHIENG, DANIEL L.
10805590	Not	41	03/19/2004	Phase alignment of audio output	CHIENG, DANIEL

	Issued			data in a multi-channel configuration	L. W.
10805591	Not Issued	80	03/19/2004	Systems and methods for sample rate conversion using multiple rate estimate counters	CHIENG, DANIEL L. W.
10805593	Not Issued	41	03/19/2004	Multi-chip PWM synchronization and communication	CHIENG, DANIEL L. W.
10805596	Not Issued	61	03/19/2004	SRC with multiple sets of filter coefficients in memory and a high order coefficient interpolator	CHIENG, DANIEL L. W.
11324132	7286009	150	12/30/2005	DIGITAL PWM AMPLIFIER WITH SIMULATION-BASED FEEDBACK	CHIENG, DANIEL L. W.
11340139	7286010	150	01/26/2006	SYSTEMS AND METHODS FOR OVER-CURRENT PROTECTION	CHIENG, DANIEL L. W.
11672191	Not Issued	41	02/07/2007	PWM Feedback/Feed-forward Protection	CHIENG, DANIEL L. W.
11672321	Not Issued	93	02/07/2007	POWER SUPPLY FEED FORWARD ANALOG INPUT FILTER COMPONENT MISMATCH CORRECTION	CHIENG, DANIEL L. W.
60615674	Not Issued	159	10/04/2004	Simulation-based feedback	CHIENG, DANIEL L. W.
10805569	7167112	150	03/20/2004	SYSTEMS AND METHODS FOR IMPLEMENTING A SAMPLE RATE CONVERTER USING HARDWARE AND SOFTWARE TO MAXIMIZE SPEED AND FLEXIBILITY	CHIENG, DANIEL L.W.
10805574	Not Issued	41	03/20/2004	Streaming multi-channel audio as packetized data or parallel data with a separate input frame sync	CHIENG, DANIEL L.W.
11672331	Not Issued	100	02/07/2007	SYSTEMS AND METHODS FOR CORRECTING ERRORS RESULTING FROM COMPONENT MISMATCH IN A FEEDBACK PATH	CHIENG, DANIEL L.W.
11782702	Not Issued	30	07/25/2007	Low-Noise, Low-Distortion Digital PWM Amplifier	CHIENG, DANIEL L.W.
11782708	Not Issued	30	07/25/2007	Digital PWM Amplifier Having a Low Delay Corrector	CHIENG, DANIEL L.W.
60456429	Not Issued	159	03/21/2003	High efficiency, high-performance sample rate converter	CHIENG, DANIEL L.W.
60469725	Not	159	05/12/2003	SRC with dual input rate estimator	CHIENG, DANIEL

	Issued			counters for automatic second sample rate detection	L.W.
60469734	Not Issued	159	05/12/2003	Multi-chip PWM synchronization and communication	CHIENG, DANIEL L.W.
60469735	Not Issued	159	05/12/2003	SRC with multiple sets of filter coefficients in memory and a high order coefficient interpolator	CHIENG, DANIEL L.W.
60469761	Not Issued	159	05/12/2003	Systems and methods for implementing a sample rate converter using hardware and software to maximize speed and flexibility	CHIENG, DANIEL L.W.
60469774	Not Issued	159	05/12/2003	Phase alignment of output audio data in a multi-SRC configuration	CHIENG, DANIEL L.W.
60469804	Not Issued	159	05/12/2003	Streaming multi-channel audio as packetized data or parallel data with a separate input frame sync	CHIENG, DANIEL L.W.

Inventor Search Completed: No Records to Display.

Search Another: Inventor

Last Name: CHIENG

First Name: DANIEL

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Inventor Name Search Result

Your Search was:

Last Name = ANDERSEN
First Name = JACK

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10329852	6741123	150	12/26/2002	DELTA-SIGMA AMPLIFIERS WITH OUTPUT STAGE SUPPLY VOLTAGE VARIATION COMPENSATION AND METHODS AND DIGITAL AMPLIFIER SYSTEMS USING THE SAME	ANDERSEN, JACK
60755560	Not Issued	159	12/30/2005	Systems amd methods for power supply tracking	ANDERSEN, JACK
60761614	Not Issued	159	01/24/2006	Systems and methods for reducing distortion and avoiding AM radio interference in a class D amplifier by adding a tone at half the switching frequency	ANDERSEN, JACK
60763614	Not Issued	159	01/31/2006	Asymmetric pulse width in 2-level full-bridge PWM output stages	ANDERSEN, JACK
60771146	Not Issued	159	02/07/2006	PWM feedback/feed-forward protection	ANDERSEN, JACK
60771147	Not Issued	159	02/07/2006	Full bridge PWM feedback analog input filter component mismatch correction	ANDERSEN, JACK
60771212	Not Issued	159	02/07/2006	Power supply feed forward analog input filter component mismatch correction	ANDERSEN, JACK
10314804	6762704	150	12/09/2002	MODULATION OF A DIGITAL INPUT SIGNAL USING MULTIPLE DIGITAL SIGNAL MODULATORS	ANDERSEN, JACK B.
10325145	6693571	150	12/20/2002	MODULATION OF A DIGITAL INPUT SIGNAL USING A DIGITAL SIGNAL MODULATOR AND SIGNAL SPLITTING	ANDERSEN, JACK B.

10328281	6925115	150	12/23/2002	APPARATUS AND METHOD FOR SAFELY HANDLING ASYCHRONOUS SHUTDOWN OF PULSEWIDTH MODULATED OUTPUT	ANDERSEN, JACK B.
10805569	7167112	150	03/20/2004	SYSTEMS AND METHODS FOR IMPLEMENTING A SAMPLE RATE CONVERTER USING HARDWARE AND SOFTWARE TO MAXIMIZE SPEED AND FLEXIBILITY	ANDERSEN, JACK B.
10805574	Not Issued	41	03/20/2004	Streaming multi-channel audio as packetized data or parallel data with a separate input frame sync	ANDERSEN, JACK B.
10805588	Not Issued	71	03/19/2004	Clip detection in PWM amplifier	ANDERSEN, JACK B.
10805589	Not Issued	93	03/19/2004	OUTPUT STAGE SYNCHRONIZATION	ANDERSEN, JACK B.
10805590	Not Issued	41	03/19/2004	Phase alignment of audio output data in a multi-channel configuration	ANDERSEN, JACK B.
10805591	Not Issued	80	03/19/2004	Systems and methods for sample rate conversion using multiple rate estimate counters	ANDERSEN, JACK B.
10805592	7078963	150	03/19/2004	INTEGRATED PULSHI MODE WITH SHUTDOWN	ANDERSEN, JACK B.
10805593	Not Issued	41	03/19/2004	Multi-chip PWM synchronization and communication	ANDERSEN, JACK B.
10805594	Not Issued	61	03/19/2004	Systems and methods for protection of audio amplifier circuits	ANDERSEN, JACK B.
10805596	Not Issued	61	03/19/2004	SRC with multiple sets of filter coefficients in memory and a high order coefficient interpolator	ANDERSEN, JACK B.
10805741	7023268	150	03/22/2004	SYSTEMS AND METHODS FOR AUTOMATICALLY ADJUSTING CHANNEL TIMING	ANDERSEN, JACK B.
10843851	7061312	150	05/12/2004	SYSTEMS AND METHODS FOR PROVIDING MULTI CHANNEL PULSE WIDTH MODULATED AUDIO WITH STAGGERED OUTPUTS	ANDERSEN, JACK B.
10843852	Not Issued	71	05/12/2004	Systems and methods for switching and mixing signals in a multi-channel amplifier	ANDERSEN, JACK B.

11324132	7286009	150	12/30/2005	DIGITAL PWM AMPLIFIER WITH SIMULATION-BASED FEEDBACK	ANDERSEN, JACK B.
11333709	7315264	150	01/17/2006	SYSTEMS AND METHODS FOR CONTROLLING TRANSIENT RESPONSE IN THE OUTPUT OF A NOISE SHAPER	ANDERSEN, JACK B.
11340139	7286010	150	01/26/2006	SYSTEMS AND METHODS FOR OVER-CURRENT PROTECTION	ANDERSEN, JACK B.
11626569	Not Issued	41	01/24/2007	Systems and Methods for Improving Performance in a Digital Amplifier by Adding an Ultrasonic Signal to an Input Audio Signal	ANDERSEN, JACK B.
11669643	Not Issued	95	01/31/2007	SYSTEMS AND METHODS FOR PULSE WIDTH MODULATING ASYMMETRIC SIGNAL LEVELS	ANDERSEN, JACK B.
11672191	Not Issued	41	02/07/2007	PWM Feedback/Feed-forward Protection	ANDERSEN, JACK B.
11672321	Not Issued	93	02/07/2007	POWER SUPPLY FEED FORWARD ANALOG INPUT FILTER COMPONENT MISMATCH CORRECTION	ANDERSEN, JACK B.
11672331	Not Issued	100	02/07/2007	SYSTEMS AND METHODS FOR CORRECTING ERRORS RESULTING FROM COMPONENT MISMATCH IN A FEEDBACK PATH	ANDERSEN, JACK B.
11782702	Not Issued	30	07/25/2007	Low-Noise, Low-Distortion Digital PWM Amplifier	ANDERSEN, JACK B.
11782708	Not Issued	30	07/25/2007	Digital PWM Amplifier Having a Low Delay Corrector	ANDERSEN, JACK B.
60456414	Not Issued	159	03/21/2003	Adaptive anti-clipping protection	ANDERSEN, JACK B.
60456421	Not Issued	159	03/21/2003	Output device switch timing correction	ANDERSEN, JACK B.
60456427	Not Issued	159	03/21/2003	Intelligent over-current, over-load protection	ANDERSEN, JACK B.
60456429	Not Issued	159	03/21/2003	High efficiency, high-performance sample rate converter	ANDERSEN, JACK B.
60469640	Not	159	05/12/2003	Multi channel PWM with	ANDERSEN, JACK

	Issued			staggered outputs	B.
60469725	Not Issued	159	05/12/2003	SRC with dual input rate estimator counters for automatic second sample rate detection	ANDERSEN, JACK B.
60469734	Not Issued	159	05/12/2003	Multi-chip PWM synchronization and communication	ANDERSEN, JACK B.
60469735	Not Issued	159	05/12/2003	SRC with multiple sets of filter coefficients in memory and a high order coefficient interpolator	ANDERSEN, JACK B.
60469760	Not Issued	159	05/12/2003	Integrated pulshi mode with shutdown	ANDERSEN, JACK B.
60469761	Not Issued	159	05/12/2003	Systems and methods for implementing a sample rate converter using hardware and software to maximize speed and flexibility	ANDERSEN, JACK B.
60469770	Not Issued	159	05/12/2003	Clip detection in PWM amplifier	ANDERSEN, JACK B.
60469774	Not Issued	159	05/12/2003	Phase alignment of output audio data in a multi-SRC configuration	ANDERSEN, JACK B.
60469776	Not Issued	159	05/12/2003	Marco PWM protection logic	ANDERSEN, JACK B.
60469787	Not Issued	159	05/12/2003	PWM output stage synchronization	ANDERSEN, JACK B.
60469804	Not Issued	159	05/12/2003	Streaming multi-channel audio as packetized data or parallel data with a separate input frame sync	ANDERSEN, JACK B.
60615674	Not Issued	159	10/04/2004	Simulation-based feedback	ANDERSEN, JACK B.
60878708	Not Issued	159	01/05/2007	Edible puzzle candy bar	ANDERSEN, JACKSON G.

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Inventor Name Search Result

Your Search was:

Last Name = HAND
First Name = LARRY

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10805569	7167112	150	03/20/2004	SYSTEMS AND METHODS FOR IMPLEMENTING A SAMPLE RATE CONVERTER USING HARDWARE AND SOFTWARE TO MAXIMIZE SPEED AND FLEXIBILITY	HAND, LARRY E.
10805588	Not Issued	71	03/19/2004	Clip detection in PWM amplifier	HAND, LARRY E.
10805590	Not Issued	41	03/19/2004	Phase alignment of audio output data in a multi-channel configuration	HAND, LARRY E.
10805591	Not Issued	80	03/19/2004	Systems and methods for sample rate conversion using multiple rate estimate counters	HAND, LARRY E.
10805596	Not Issued	61	03/19/2004	SRC with multiple sets of filter coefficients in memory and a high order coefficient interpolator	HAND, LARRY E.
10843852	Not Issued	71	05/12/2004	Systems and methods for switching and mixing signals in a multi-channel amplifier	HAND, LARRY E.
11211765	7259618	150	08/25/2005	SYSTEMS AND METHODS FOR LOAD DETECTION AND CORRECTION IN A DIGITAL AMPLIFIER	HAND, LARRY E.
11324132	7286009	150	12/30/2005	DIGITAL PWM AMPLIFIER WITH SIMULATION-BASED FEEDBACK	HAND, LARRY E.
11340139	7286010	150	01/26/2006	SYSTEMS AND METHODS FOR OVER-CURRENT PROTECTION	HAND, LARRY E.
11782702	Not Issued	30	07/25/2007	Low-Noise, Low-Distortion Digital PWM Amplifier	HAND, LARRY E.

11782708	Not Issued	30	07/25/2007	Digital PWM Amplifier Having a Low Delay Corrector	HAND, LARRY E.
60456414	Not Issued	159	03/21/2003	Adaptive anti-clipping protection	HAND, LARRY E.
60456422	Not Issued	159	03/21/2003	Output filter, phase/timing correction	HAND, LARRY E.
60456427	Not Issued	159	03/21/2003	Intelligent over-current, over-load protection	HAND, LARRY E.
60456428	Not Issued	159	03/21/2003	Output filter speaker/load compensation	HAND, LARRY E.
60456429	Not Issued	159	03/21/2003	High efficiency, high-performance sample rate converter	HAND, LARRY E.
60456430	Not Issued	159	03/21/2003	Frequency response correction	HAND, LARRY E.
60469725	Not Issued	159	05/12/2003	SRC with dual input rate estimator counters for automatic second sample rate detection	HAND, LARRY E.
60469735	Not Issued	159	05/12/2003	SRC with multiple sets of filter coefficients in memory and a high order coefficient interpolator	HAND, LARRY E.
60469761	Not Issued	159	05/12/2003	Systems and methods for implementing a sample rate converter using hardware and software to maximize speed and flexibility	HAND, LARRY E.
60469762	Not Issued	159	05/12/2003	PWM software protection schemes	HAND, LARRY E.
60469770	Not Issued	159	05/12/2003	Clip detection in PWM amplifier	HAND, LARRY E.
60469774	Not Issued	159	05/12/2003	Phase alignment of output audio data in a multi-SRC configuration	HAND, LARRY E.
60969608	Not Issued	20	09/01/2007	Systems and Methods for HDA Codec with Integrated Class-D PWM Controller to Handle HDA Volume Control	HAND, LARRY E.
60969609	Not Issued	20	09/01/2007	HDA Communication between the Application and the DSP in a HDA Audio Codec for Local Intelligent Processing	HAND, LARRY E.
60969614	Not Issued	20	09/01/2007	Intelligent "Mode Control" Using Plug-In Personalities	HAND, LARRY E.
60969615	Not	20	09/01/2007	Scalable Output Configurations	HAND, LARRY E.

	Issued			for Smart Amplifiers	
60988365	Not Issued	20	11/15/2007	Switching Amplifier Optimized for Minimal and Stable Output Semiconductor Dead Times	HAND, LARRY E.
06643315	4600891	150	08/21/1984	DIGITAL AUDIO AMPLIFIER HAVING A HIGH POWER OUTPUT LEVEL AND LOW DISTORTION	HAND, LARRY E.
06643316	4611300	150	08/21/1984	DIGITAL DELAY LINE	HAND, LARRY E.
06874379	4724396	150	06/13/1986	DIGITAL AUDIO AMPLIFIER	HAND, LARRY E.
07211217	RE33333	150	03/11/1988	DIGITAL AUDIO AMPLIFIER HAVING A HIGH POWER OUTPUT LEVEL AND LOW DISTORTION	HAND, LARRY E.
07422518	4992751	150	10/17/1989	AUDIO AMPLIFIER WITH PHASE MODULATED PULSE WIDTH MODULATION	HAND, LARRY E.
09365019	6239655	150	08/02/1999	MICROPHONE AMPLIFIER WITH DIGITAL GAIN CONTROL	HAND, LARRY EUGENE
60128305	Not Issued	159	04/08/1999	MICROPHONE AMPLIFER WITH DIGITAL CONTROL	HAND, LARRY EUGENE
60380029	Not Issued	159	05/02/2002	System and process for detection of weak or non-functioning cylinders in engines	HANDLER, LARRY
10108971	6802221	150	03/27/2002	SYSTEM AND METHOD FOR CONDITIONED-BASED MONITORING OF A BEARING ASSEMBLY	HANDLER, LARRY R.
10158750	Not Issued	161	05/30/2002	System and method for conditioned based monitoring using acoustic diagnosis	HANDLER, LARRY R.
10159512	6985803	150	05/30/2002	SYSTEM AND METHOD FOR MONITORING THE CONDITION OF A VEHICLE	HANDLER, LARRY R.
60279650	Not Issued	159	03/29/2001	Automatic analysis and detection of faults	HANDLER, LARRY R.
60294330	Not Issued	159	05/30/2001	Automated smart underpass system for predictively monitoring and early determining the condition of land-based transportation assets	HANDLER, LARRY R.
60294354	Not	159	05/30/2001	Condition based monitoring for	HANDLER, LARRY

	Issued			land-based equipment	R.

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